Eric Deal

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Experience:

Ambiq Micro

Senion Design Engineer November 2014-present

- Responsible for microarchitecture and design of several portions of Ambiq's two most recent MCU generations
  - Architecture, design, and partial verification of flash cache, flash, SRAM, DMA, and multi-bit SPI modules
  - Re-architected internal bus/peripheral/clocking structure to address bottlenecks in design/timing closure in near-thrseshold (SPOT) design
  - Developed creative design techniques to minimize power while addressing the unique characteristics of near-threshold design
- Developed Ambiq's MCU hardware validation environment
  - Developed FPGA design used to control validation board and exercise MCU hardware
  - Developed flexible, scriptable, object-oriented, Linux-based C/TCL environment to control validation environment
  - Implemented SQL-based database environment and PHP code to log, analyze, and report hardware regression data
- Developed internal tools to automate design and implementation
  - Implemented backend Innovus procedures to address setup/hold issues the tools couldn't natively fix (large multi-corner analysis)
  - Implemented an SQL database to correlate results from multi-corner timing analysis to identify timing issues across large number of PVT corners
  - Created Perl script to manage simulation/synthesis/FPGA file list generation
  - It's more fun to automate a repetitive task than do it again by hand

Cyclic Design

President/Consultant May 2009-present

- Formed Cyclic Design to provide hardware design consulting and IP licensing, specializing in NAND Flash error correction and controllers.
- Handled all tasks related to design, verification, marketing, and sales of BCH IP. Significant IP includes
  - G12: ECC 2-16 over 256 bytes,
  - G13/G13X: ECC 2-64 over 512 bytes,
  - G14/G14X: ECC 2-96 over 1024 bytes,
  - G15: ECC2-96 over 2KB
- Various contracts to customize BCH IP and provide general design services

MultiXtor

Founder/VP Hardware Engineering June 2008-August 2009

- Founded high-performance enterprise storage startup with two former colleagues from Sigmatel.
- Architected and implemented all hardware aspects of our product, from high-level architecture to verilog design/verification and implementation in an FPGA.
- Developed both C++ reference model and verilog BCH ECC design with many optimizations to the algorithm to minimize area consumed in the FPGA.
- Developed initial high-level C++ model of our system that enabled us to model the performance of the design.
- Performed many other roles such as system/network admin, marketing, accountant, purchasing, and white-board hanger.

Sigmatel/Freescale Personal Systems Group

Digital Design Engineer-IC5 (Freescale) April 2008-June 2008

Principle Member Technical Staff December 2005-March 2008

- Provided significant direction in chip-level architecture for most recent audio/video chips at Sigmatel to ensure that the designs are robust enough to support system-level requirements.
- Developed AXI infrastructure for portions of three designs. Retrofitted AXI into a derivative chip to enable higher video performance, implemented AXI bridge/interfaces for several legacy blocks, and implemented a 4:1 AXI fabric that included address translation capabilities for virtual memory support.
- Proposed framebuffer rotation/blending engine that became the basis for a low-area pixel rendering subsystem. I architected the block, split design duties with another engineer, and developed an image-based verilog testbench to test a significant portion of the design.
- Designed a BCH-based ECC block to supercede the former Reed-Soloman (RS) ECC block. Designed the syndrome/parity generation logic and Chien Search logic from scratch and used a modified version of the KES block from the RS ECC block.
- Took over redesign of key equation solver (KES) portion of an 8-symbol ECC correction block for NAND flash interface. The interface previously supported 4-symbol correction and was being redesigned to support 4/8 symbol correction and rearchitected to minimize CPU overhead. Replaced the existing Euclid-based KES algorithm with a Berlekamp-Massey based implementation and updated Chien-Search Forney-Evaluator (CSFE) module to support 8-symbol correction.
- Architected and implemented a data processing module that originally was intended to perform encryption operations but also assumed several other data processing tasks to offload the system processor. Implemented AES-128 algorithm (with ECB and CBC modes), SHA-1 and CRC32 hash algorithms, memory copy functions (to assist processor in virtual memory management), rudimentary blit/fill operations, and a colorspace converter. The design was architected for minimal area by sharing resources and making design tradeoffs that favored area over performance.

Conexant Systems/Rockwell International, Broadband Media Processing Division

Principle Design Engineer January 2003-October 2005
Senior Staff Design Engineer January 2000-January 2003
Staff Design Engineer September 1998-January 2000
Senior Design Engineer November 1996-September 1998

- Designed system-level components and architecture for four generations of MPEG set-top box SOCs including bus structures, processor, peripherals, and external IO interfaces.
- Developed the HSX bus protocol to accomodate the internal system bus requirements of our SOCs. The protocol implements tagged split transaction controls to maximize bus utilization and allow for high memory controller efficiency. The protocol was also designed to scale well with both frequency and bus segment sizes and implements an area-efficient shared-address bus and data crossbar switch. Implemented interface modules to simplify peripheral connection to the bus that allowed for timing/protocol changes without requiring changes to peripheral RTL.
- Developed an all-digital DDR physical layer interface for our memory controllers that allowed us to port our memory controller via synthesis to different processes without having to create new analog blocks. The interface performed the DLL functionality and included control logic to automatically create the quarter-cycle delays required for DDR operation. Worked in Magma with our layout engineer to ensure valid timing and skew requirements.
- Design responsibilities included interfaces for off-chip PCI, ISA/Flash, Parallel-ATA, and smartcard devices as well as on-chip designs for processor interface, DMA, encryption, clock generation, system control, and other minor peripherals. The PCI/ISA design used shared pins to minimize pin count but still allow for full functionality of both busses. The PCI interface also operated in both bridge and device mode so that we could operate the same chip in both environments.
- Responsible for chip-level simulation environment for the first three generations of our chips and helped guide our verification group's development of an advanced environment for our fourth generation chips. Found creative solutions to improve simulation performance and managed regressions while also performing design responsibliities.
- Developed new tools and processes to aid in design/verification and brought in third-party tools to aide in development. I was one of the first to use Linux as an engineering desktop and built a powerful, cost-efficient Linux server farm to supplement our Sun machines as the various EDA tools became available on Linux. Developed tools to improve design methodology and timing analysis.

IBM, RS/6000 Workstation Division

Senior Associate Engineer October 1995-October 1996
Associate Engineer January 1993-October 1995

- Designed a high-performance PCI interface for our group's memory-I/O controller. The chip contained two PCI bridges: a 32-bit, 33 MHz PCI bridge and a 64-bit, high-performance PCI bridge. Both PCI bridges utilized common logic synthesized to the specifications of the individual target bridges.

- Created an object-oriented simulation environment based on C++ which provided multi-tasking capabilities and encapsulation of the simulation interface with C++ objects. This environment allowed for the creation of separate behavioral models to emulate the function of various devices, each of which could be configured at run-time without recompilation. Taught other design groups how to utilize our simulation environment and continued to support and enhance the environment as the sophistication of the simulation objects increased.
- Wrote C++ behaviorals of the PowerPC 604 and 601 processors, a generic PCI-compliant master/slave behavioral, L2 look-aside caches, and several chip-specific behaviorals.
- Wrote and maintained numerous tools for our design group and general use within IBM.

Tools, Languages, Skills, and other interests

- Verilog, Tcl/Tk, C/C++, PHP, MySQL, Perl, HTML, CSS
- VCS, Magma, Debussy/Verdi, Cadencesynthesis, and various other EDA tools
- FPGA development: experience with Altera, Xilinx, familiar with other FPGAs
- Interests include photography, cycling, Linux, PHP/MySQL, and sustainable living

Education:

Texas A&M University, B.S. in Electrical Engineering, Magna Cum Laude, December 1992.